Exhibit A

ATTACHMENT A

Professor Woodward Yang's Expert Disclosure

I. INTRODUCTION

Fujian Jinhua Integrated Circuit Company, Ltd. ("Jinhua") hereby provides notice of its intent to introduce expert testimony from Professor Woodward Yang, pursuant to Federal Rules of Evidence 702, 703 and 705. This disclosure is made pursuant to Rule 16(b)(1)(C) of the Federal Rules of Criminal Procedure, which provides that when the government makes an expert disclosure pursuant to Rule 16(a)(1)(G), the defendant must make a reciprocal disclosure that includes "a written summary of any testimony that the defendant intends to use" which "describe the witness's opinions, the bases and reasons for those opinions, and the witness's qualifications."

Jinhua's counsel asked Professor Yang to examine the technical documents produced in this case and the expert disclosures by the government's purported experts Terrence Daly and Thomas Dyer (dated July 2, 2021), and to provide his expert understanding and opinion on the following topics among others:

- A general background on Dynamic Random Access Memory ("DRAM"), how it functions, and its cell structure;
- A high-level overview of how DRAM is manufactured and designed;
- A description of the DRAM industry during the relevant time period;
- Prof. Yang's analysis of the technical documents produced by the government, including the documents that the government has identified as Trade Secrets 1 through 8, which Prof. Yang will sometimes refer to as Alleged Trade Secrets 1 to 8 (or simply "ATS 1," "ATS 2," etc.);
- Prof. Yang's opinion on whether:
    - Micron Technology, Inc. (Micron) and the companies it acquired, Rexchip and Elpida, took reasonable measures to keep ATS 1-8 secret;
    - The information contained in ATS 1-8 was generally known to or readily ascertainable through proper means, and whether it would have independent economic value to United Microelectronics Corporation ("UMC") and Jinhua;
- Professor Yang's analysis of whether he saw any evidence in the technical documents produced by UMC and the government that UMC was trying to copy or replicate, either exactly or in any substantial part, the DRAM design, process flows or other technical information reflected in ATS 1 through 8; and
- Whether the development timeline proposed in the Technology Cooperation Agreement between UMC and Jinhua appeared reasonable for UMC to achieve based on independent development.

Jinhua's and Professor Yang's factual investigation and trial preparation is ongoing, and Jinhua reserves the right to supplement Professor Yang's expert disclosure as appropriate.

II. BACKGROUND AND QUALIFICATIONS

Professor Yang is currently the Gordon McKay Professor of Electrical Engineering and Computer Science in the School of Engineering and Applied Science at Harvard University, where he has taught and pursued research endeavors since 1990. In particular, Prof. Yang has taught graduate and undergraduate level courses in computer architecture, computing hardware, digital logic design, mixed signal circuit design, circuit theory, and engineering design which are related to and involve the design, analysis, and manufacture of microelectronic circuits such as microprocessors and DRAM.

Professor Yang's academic research pursuits have been directed to the development of advanced computing and memory systems for high performance computing systems and integrated sensor and computing systems. Prof. Yang's research has been primarily supported and funded by the National Science Foundation, the Army Research Office, DARPA, and Samsung Electronics. He has received numerous honors and awards for his contributions to the electrical engineering industry, including the National Science Foundation Young Investigator Award, Army Young Investigator Award, Hertz Foundation Fellowship, and National Science Foundation Fellowship.

Professor Yang was appointed to be a Harvard Business School ("HBS") University Fellow due to his expertise and experience with high technology industries and is also the founding faculty director of the Master in Design Engineering Program at Harvard University which combines the disciplines of engineering, business, and design to solve complex, real world problems. In this capacity, Prof. Yang has also conducted research and taught courses on the commercialization of new technologies, technological innovation, business economics, and industry architecture.

Professor Yang also has extensive industrial experience working with various companies in the semiconductor and electronics industries. From 1995 to 2000, he worked as a consultant and Senior Fellow at Hyundai Electronics Industries (now known as SK Hynix), in Ichon, Korea. At Hyundai, he pursued advanced research on the design and manufacture of Dynamic Random Access Memory ("DRAM") and merged memory logic ("MML") technology for advanced computer systems including the development of a high performance CMOS image sensor technology which was based on a DRAM manufacturing process.

From 2000-2008, Professor Yang founded and led a fabless DRAM design company (Silicon7) in Korea, Taiwan, and China which was involved in the design, manufacture, testing, packaging, marketing, and sales of ultra-low power DRAM and other specialized memory products to large electronics manufacturers such as Samsung, Motorola, and LG. As the CEO of Silicon7, Prof. Yang was also a member of the Fabless Semiconductor Alliance ("FSA"), which promoted and advocated for businesses involved in the design, manufacture, testing, packaging, and sales of semiconductor products using the "fabless business model."

A more detailed record of Professor Yang's professional qualifications, including a list of publications, awards, and professional activities, as well as cases in which he has testified as an expert at trial or in depositions is set forth in his Curriculum Vitae, which is attached hereto as Exhibit 1. Jinhua has compensated Prof. Yang at his standard professional rate of $800 per hour.

III. DESCRIPTION OF MATERIALS PROFESSOR YANG REVIEWED

Jinhua's counsel gave Professor Yang access to the entire database of discovery produced by the government in this case, including the technical documents produced by the government, the documents from the so-called "Taiwan Drive" (files from the 26 seized devices during Taiwanese law enforcement's raids on UMC's Tainan office on 02/07/2017 and 02/14/2017), transcripts of witness statements, testimony and FBI FD-302s, and various court filings from this case, including the Indictment. Due to the voluminous size of the database, which includes roughly 6 million documents (more than 18 million pages), Jinhua's counsel provided a selection of relevant documents to Prof. Yang, but he had the ability to search the entire database. In addition, Prof. Yang conducted independent research and reviewed numerous articles, treatises and patents in the public record.

A complete list of the materials that Professor Yang considered is attached hereto as Exhibit 2.

IV. PROF. YANG'S UNDERSTANDING OF FEDERAL STATUTE AT ISSUE (18 USC 1839(3))

Professor Yang understands that, in order for information to constitute a "trade secret" under 18 U.S.C. § 1839(3): (1) the owner thereof must have taken reasonable measures to keep such information secret, and (2) the information must derive independent economic value, actual or potential, from not being generally known to, and not being readily ascertainable through proper means by, another person who can obtain economic value from the disclosure or use of such information. *See* 18 U.S.C. § 1839(3). Professor Yang understands that when determining whether the information derives independent economic value from being kept secret, courts consider the degree, if any, to which the secret information confers a competitive advantage. *See* United States v. Chung, 659 F.3d 815, 826 (9th Cir. 2011).

Professor Yang also understands that information does not constitute a "trade secret" under 18 U.S.C. § 1839(3) if the use or disclosure of such information would provide no actual or potential economic value to another, either because such information is generally known or readily ascertainable through proper means. *See* 18 U.S.C. § 1839(3). Professor Yang further understands that reverse engineering is one of those proper means by which one can lawfully obtain information that another may attempt to keep secret.

V. SUMMARY OF EXPERT OPINIONS AND EXPECTED TESTIMONY ABOUT DRAM AND DRAM INDUSTRY

A. Background on DRAM, DRAM Design and DRAM Industry

Professor Yang will testify about the function and role of DRAM, explain basic details about the major components and design of DRAM chips, briefly discuss how DRAM is designed and manufactured, and provide some high-level detail on the DRAM industry.

1. Where and How is DRAM Used?

While computers and mobile smart phones make use of powerful microprocessors, all modern digital computing devices also require vast amounts of memory to store programs and associated data. There are usually three types of digital memory that are used. SRAM ("Static Random Access Memory") is typically integrated into the processors to serve as a high speed memory cache. Dynamic Random Access Memory ("DRAM ") is used for main memory since it is considerably less expensive than SRAM, but is significantly slower. Finally, hard disk drives and solid-state storage drives are used for long term non-volatile memory storage when the device is powered off.

2. How Does a DRAM Cell Function?

DRAM is based on a one-transistor, one-capacitor ("1T1C") cell structure and circuitry, which was patented over fifty years ago (U.S. Patent No. 3,387,286 to Dennard, issued June 4, 1968). The DRAM cells are arranged in an array with many rows and columns. By storing electrical charge on the capacitor as a high or low voltage, data "1" or "0" is stored in the DRAM cell. Over time, the charge in the capacitor will leak/discharge, so the data in the DRAM needs to be periodically refreshed.

3. What Are the Major Components of a DRAM Product?

While the DRAM cell provides the memory storage of a digital bit, other significant structures and circuitry are also required to make a complete DRAM product. These would include appropriate structures and interface circuitry at the periphery of DRAM cell arrays such as sense amplifiers, wordline drivers, address decoders, dummy DRAM cells to improve yield, voltage bias generators, and high speed physical interfaces. In addition, commercially viable DRAM products would also need to include repair circuitry to allow the replacement of defective DRAM memory cells through the use of programmable fuses with spare DRAM cells and possibly built-in test circuitry. All of these components are necessary to realize a complete DRAM product.

4. Key DRAM Cell Device Structures

Starting as early as 2001, but no later than approximately 2014, the structure of advanced DRAM cells were well known to incorporate Shallow Trench Isolation for the Active Area, Buried Wordline with recessed access transistors, subsequent Bitline (aka Digitline) above the Wordline, and specialized contact structures between the access transistor and Storage Capacitors which are situated in a tightly packed array above the access transistors. (*See* U.S. Patent Nos. 7613025B2 (2008); 7349232B2 (2008); 8519462B2 (2011); 8508982B2 (2011); U.S. Patent Application Publication Nos. 2014/0145268A1 (2012); 2014/0154882A1 (2012)). These advanced DRAM cell structures were also known to make use of a 6F2 layout in an open bitline architecture. The 6F2 layouts also typically made use of Active Areas that were "tilted" in order to facilitate tighter packing.

5. How is a DRAM product designed and manufactured?

DRAM products are composed of multiple major components as described above which have interdependencies in their specifications and designs. In particular, this means that it is not

practical to simply extract and change component specifications and designs since changes to one component typically force a cascade of adjustments.

The device structure of the DRAM cell and array is highly dependent on the detailed sequence of process steps and related photomask patterns to achieve the desired 3D DRAM cell structure. Even apparently minor changes in the thickness of material layers or width structures can have drastic impacts on the functionality, performance and yield of DRAM. Even small differences in the configuration of semiconductor manufacturing equipment from different suppliers can also cause major problems. This type of highly interdependent process requires detailed hand customization and optimization. Simple copying of process recipes and structure shapes is highly unlikely to yield satisfactory technical device structure or array results.

Designing DRAM periphery interface circuitry also must be specifically tailored and optimized to the physical and electrical specifications of the DRAM cell, array and the desired overall performance of the DRAM product. The final DRAM chip design consists of the synthesis of the DRAM cell, array and DRAM periphery interface circuitry. However, that specific DRAM chip design is also intimately linked to the specific detailed manufacturing process which oftentimes is changed to further optimize or improve the performance and/or yield of the DRAM chip.

The detailed manufacturing process for DRAM typically consists of many hundreds of detailed steps which are specific not only to the DRAM cell, array and the DRAM periphery interface circuitry, but also to the specific manufacturing equipment that is being used. However, that overall semiconductor wafer manufacturing process for DRAM can be basically categorized into 4 important types of processing steps:

- Photolithography, which consists of applying a photosensitive chemical to the wafer and exposing a light pattern on the wafer such that a patterned material is left on the wafer;
- Deposition/Diffusion, which consists of depositing or creating the formation of a layer of material on top of the wafer by chemical reaction and/or physical deposition. Formation of material layers will depend on the specific characteristics of the deposition mechanisms and underlying structures;
- Etch, which consists of removing material from the top of the wafer by chemical and/or physical methods. Some materials may be preferentially removed or left intact due to the composition or physical orientation; and
- Ion Implantation, which consists of accelerating ionized atoms of specific elements directly into the wafer. Some ionized atoms will be incorporated into the silicon lattice while other atoms may be effectively shielded from entering the silicon lattice due to intervening structures.

Advanced semiconductor manufacturing also requires a great deal of more routine steps including:

- Cleaning, which consists of various liquid and gas chemical baths to remove contaminants since the smallest particles can disrupt the successful manufacturing and functionality of these microelectronic devices; and

- Metrology, which consists of various measurements on the wafer to make sure that the proper intermediate results were achieved by processing steps.

The specific details for each of the hundreds of processing steps represents the optimized conditions for a specific DRAM chip which is composed of a specific DRAM cell and array and DRAM periphery interface circuitry, and is based on specific semiconductor manufacturing equipment. The specific details of each processing step for an existing DRAM chip based on a specific set of semiconductor manufacturing equipment would be of limited economic value to someone manufacturing a DRAM chip based on a significantly different DRAM cell and using a different set of semiconductor manufacturing equipment.

Finally, after the silicon wafer finishes the manufacturing process, every one of the hundreds or thousands of DRAM chips on that silicon wafer must be extensively tested under many different conditions, defective DRAM cells must be repaired, and each functioning DRAM chip must be appropriately cut out of the wafer and usually put into a standardized JEDEC (Joint Electron Device Engineering Council) package. The technical and manufacturing challenges for testing, repair, and packaging of DRAM products are significant and nontrivial and are necessary for a successful DRAM manufacturing operation.

6. History of DRAM Device Structures

a. Planar Cell vs. Stacked Cell vs. Trench Cell

DRAM cell structure and layout has evolved significantly over the last 50 years. In the 1970's, the original DRAM cell structures used a planar (flat) DRAM cell structure. In 1977, the invention of a stacked DRAM cell structure allowed for denser and more efficient DRAM by stacking the storage capacitor above the DRAM access transistor and which made the planar DRAM cell obsolete. Alternatively, in the early 1980's, some companies pursued a trench DRAM cell structure which allowed for smaller DRAM cells by forming the storage capacitor in a deep trench in the silicon substrate underneath the DRAM cell. Eventually, the stacked DRAM cell structure proved to be more effective as all major DRAM manufacturers abandoned trench DRAM cell structures around 2010.

b. 8F2 Cell to 6F2 Cell

In the continual effort to make smaller and more efficient DRAM cells, the DRAM cell structure evolved from a rectangular shaped DRAM cell that was roughly 8F2 in area (*i.e.*, 4F x 2 F where F was nominally the smallest semiconductor feature that could be manufactured) to a tilted parallelogram shaped DRAM cell that was smaller (about 6F2 in area) starting around 2001. This smaller 6F2 DRAM cell required an open bit line array architecture compared to a folded bit line bit array architecture used for the larger 8F2 DRAM cell. This effort was similarly accompanied by an effort to reduce the size of the DRAM access transistor by pursuing a recessed transistor structure that is now commonly called Buried Wordline. Major DRAM manufacturers abandoned 8F2 for 6F2 DRAM cell structures around 2010.

c. 3x2 6F2 cell vs 2x3 6F2 cell

As DRAM cells became smaller, there were increasing problems with the proper functioning and smooth manufacturing of DRAM. 3x2 6F2 DRAM cell structure required greater precision in manufacturing silicon structures but offered superior electrical performance. 2x3 DRAM cells structures could be manufactured with more relaxed spacings but offered inferior electrical performance. Samsung and SK Hynix aggressively pursued the 3x2 6F2 DRAM cell structure while Elpida and Micron initially pursued the 2x3 DRAM cell structure. Currently, the 3x2 6F2 DRAM cell structure is now dominant as Micron recently abandoned the 2x3 6F2 DRAM cell structure.

7. Integrated Device Manufacturers and Foundries in the Semiconductor Industry

Originally, almost all semiconductor manufacturers were Integrated Device Manufacturers (IDMs) which processed semiconductor wafers as well as designed the semiconductor chips. Intel is one of the most prominent examples of an IDM. Samsung, SK Hynix, and Micron are examples of DRAM IDMs. However, due to the rising complexity for both designing and manufacturing, foundries that only focused on semiconductor manufacturing started to emerge. Foundries worked closely with design houses that design complex semiconductor chips which the foundry would manufacture. TSMC and UMC are two examples of large semiconductor foundries. Qualcomm, Marvell, and Apple are examples of large companies that design semiconductor chips for manufacturing at TSMC and UMC. There are also many smaller companies that design complex semiconductor chips. In addition, Samsung has started to offer foundry services with Intel also recently announcing its intent to enter this type of business.

Historically, the foundry business has been mostly focused on logic products such as microprocessors. However, there have also been foundries which could produce memory products such as DRAM or Flash. ESMT (Elite Semiconductor Memory Technology or EliteMT) and Etron are two examples of design companies that design DRAM for fabrication at foundries. During the late 1990s to early 2000s, UMC provided DRAM foundry services.

8. Semiconductor Manufacturing Process Technologies for Logic and DRAM

Logic and DRAM semiconductor manufacturing technology are roughly based on the same general techniques, well-known principles, and for the most part the same type of equipment. The primary difference is the Logic semiconductor manufacturing process is optimized for high speed and low power transistor performance, while the DRAM semiconductor manufacturing process is optimized to make low leakage and very small transistors and capacitors for DRAM cells.

With the recent emergence of the 6F2 stacked DRAM cell and well established advanced semiconductor manufacturing equipment and techniques, it has become relatively easier for foundries with logic semiconductor manufacturing technology to pursue the development of advanced DRAM. In particular, the 6F2 stacked DRAM cell has many structural similarities to an embedded DRAM cell structure with a stacked storage capacitor above both the access transistor and bitline which was patented by UMC in 2002. (*See* U.S. Patent No. 6,406,971 (2002)).

9. What is Reverse Engineering?

Reverse engineering is the process of deconstructing and analyzing a semiconductor product to determine the device structure, electrical circuits, subcomponents, overall performance, manufacturing process used, manufacturing costs, etc. It is regularly and widely performed throughout the semiconductor industry. Reverse engineering a product that has been released for sampling or for sale to the public is considered a proper means of gleaning information. Information that can be gleaned from reverse engineering a product that is available to the public is considered properly accessible and therefore cannot be considered a legitimate trade secret. There are many legitimate, specialized companies that provide these reverse engineering services. TechInsights is one of the largest and most famous in the semiconductor and electronics industries. For example, they are well known for their "tear down analysis" of Apple iPhones.

B. DRAM Industry Primer

Professor Yang will testify that around 2015, there were three major competitors in the DRAM market: Samsung, Hynix and Micron. Of these three, Samsung was the largest and was generally seen as producing among the most advanced DRAM chips, followed by SK Hynix in second and Micron in third. Samsung controlled slightly more than 40% market share, with SK Hynix and Micron at roughly 26% and 24% respectively. Semiconductor manufacturing processes are generally characterized by their "feature size" measured in nanometers ("nm"). Smaller feature sizes correspond to more advanced processes that result in greater memory capacity per chip area. As of late 2015, the majority of DRAM production for Samsung, SK Hynix and Micron were at roughly 20nm, 21nm, and 25nm respectively, with 14nm DRAM emerging as the latest technology in the field.

The DRAM cell structures produced by Samsung, SK Hynix, and Micron all incorporated similar features such as 6F2 cells with buried wordlines and large stacked capacitors. (*See, e.g.,* TAIWANHD-00000699, a TechInsights April 2015 report indicating that Samsung and Hynix appeared to be ahead of Micron in technology and in market share.) While these companies were in direct competition there was also significant cooperation in defining appropriate open industry standards through organizations such as JEDEC and IEEE. Furthermore, the entire industry of semiconductor equipment manufacturers was also competing and cooperating through organizations such as ITRS (International Technology Roadmap for Semiconductors), which attempted to coordinate the development of next generation semiconductor technology by sharing information between semiconductor manufacturers such as Samsung and Micron with equipment manufacturers such as Applied Materials and Tokyo Electron.

VI. SUMMARY OF EXPERT OPINIONS ON SPECIFIC FACTS IN THE CASE

A. The General Concepts, Cell Structure And Overall Process Sequence Reflected In ATS 1 Through 8 Are All Generally Known And Readily Ascertainable.

Professor Yang will testify that the high-level DRAM structures, manufacturing process flows, and design rules described in ATS 1-8 were well-known in the DRAM industry during the relevant time frame (2015-2017). The one-transistor, one-capacitor (1T/1C) DRAM cell was

invented over fifty years ago, and subsequent developments are extensively documented in textbooks, technical papers, the trade press (*e.g.*, EE Times, EDN), and market analysis reports. DRAM manufacturers present their latest technology every year at widely attended conferences such as IEDM (Internal Electron Devices Meeting) and ISSCC (International Solid-State Circuits Conference), which include detailed tutorials and courses in addition to presentations of technical papers. Because commercial DRAM chips are routinely reverse engineered by competitors and third parties, the DRAM industry relies heavily on patents to protect their innovations. As a result, patents provide timely and detailed information concerning the structure and manufacturing processes employed by major DRAM manufacturers such as Samsung, Hynix, and Micron. (*See* KR20160015783A; KR20160015783A; US 6,423,474; KR20130078965A; US20090008714A1 as a representative set of examples.) As a result, Professor Yang will testify that not only is the general structure of DRAM products well known, but the overall sequence of manufacturing steps is generally known in the industry. For example, it is common knowledge that shallow trench isolation ("STI") is performed before forming a buried wordline ("BWL"). Thus, for instance, the general cell structure and general process flow for Micron's 25nm DRAM chip as reflected in ATS 1-5, was well known and readily ascertainable well before the alleged trade secret documents were allegedly misappropriated in this case.

Professor Yang will testify that at a high level, the overall concepts and techniques for fabricating a DRAM product based on 6F2 stacked DRAM cell structure were generally well known in the industry from relevant patents, published literature, and reverse engineering. Semiconductor fabrication is necessarily composed of sequential steps, and it is commonly understood that layers that are below need to necessarily precede layers that are above. Therefore, the fabrication sequence can be deduced through careful analysis of device structures. To the extent that temporary layers might not be present in the final DRAM device structures and therefore may not be directly observable by reverse engineering, those temporary layers will necessarily leave an ascertainable mark in the device structures. Furthermore, the techniques and necessity for temporary layers are well known (e.g. Self-Aligned Double Patterning).

Professor Yang will testify that DRAM research is performed not only by the DRAM manufacturers themselves, but also by entities that make the results of their research widely available to industry players. For example, semiconductor equipment manufacturers such as Applied Materials ("AMAT"), Tokyo Electron ("TEL"), LAM Research, and ASML routinely provide all of their customers with Best Known Methods ("BKMs") or optimized recipes to use their products, such that customers do not have to develop their own recipes from scratch. Many DRAM innovations are the result of academic research which is widely and openly disseminated. Detailed DRAM standards and specifications are openly and collaboratively disseminated by organizations such as JEDEC and IEEE. Overall technology planning around materials, techniques, and equipment are openly discussed and provided in organizations such as ITRS.

Professor Yang will testify that the vast majority of information regarding the structure and manufacturing process of a DRAM product, including the DRAM structures and manufacturing processes depicted in ATS 1-8, can be obtained through reverse engineering. Reverse engineering of DRAM chips is widely accepted and legally permissible in the semiconductor industry, including the DRAM industry. Such reverse engineering is regularly performed both in-house by leading DRAM manufacturers, and by independent firms that reverse-engineer new products as

soon as they hit the market and offer detailed reports for sale. Indeed, Micron's 25nm DRAM chips were reverse engineered during the relevant time period by TechInsights and Chipworks. (*See e.g.,* TAIWANHD-00000699; TAIWANHD-00000701.) It is standard practice for semiconductor manufacturers to purchase such reports in order to keep abreast of the competition. Information available from reverse engineering reports includes high-resolution images down to atomic detail as obtained by SEM and TEM imaging techniques; accurate dimensional measurements of every physical feature, such as the thickness of various layers; chemical analysis as obtained from, *e.g.*, SIMS, SEM-EDS, and TEM-EDS techniques; the overall manufacturing process flow, as obtained from analyzing the unique signatures of deposition and etch steps; critical spacings (*i.e.*, design rules); and detailed circuit extraction for all of the important circuit blocks such as sense amplifiers and wordline drivers.

Professor Yang may testify that, at the level of general concepts and overall understanding, what one finds in ATS 7 and ATS 8 was already well known in the industry as documented by many technical publications, reverse engineering of similar products, and patents, which are all in the public domain. To the extent ATS 7 and ATS 8 *might* have some details that one would not find in a patent, Prof. Yang will testify that those details are Micron-specific, and would have had little value to a competitor that was not seeking to replicate Micron's specific 3x2 1xnm DRAM cell structure. More importantly, prior to 2015, the general concepts and techniques for even more advanced 14nm DRAM structures were already being publicly discussed and circulated, and were readily gleaned from public source documents such as academic papers and even some reverse engineering reports.

Relatedly, Professor Yang will testify that many of the Alleged Trade Secrets appear to be general training documents meant for training equipment operators, technicians, and junior engineers. For example, on page 4 of ATS 7, the document itself clearly states that it is "for: learning major concepts," "a general exposure" to Micron's 110 Series flow, and "understanding how electrical and physical structures are built and why." (*See* USD-0560710 at 4.) The face of the document tells the reader that ATS 7 "is *not* for: critical dimensions, measurements, target values" or for "determining specific toolsets" or even for "site-to-site comparison." (*Id.*) Thus, Micron itself makes clear that ATS 7 is only meant to convey basic information about Micron's 110 Series DRAM, and is not meant to convey any "critical dimensions, measurements, target values" (*id.*) or other key information about the DRAM technology. Prof. Yang will testify that companies interested in preserving highly confidential and valuable trade secrets would generally hold those documents closely and would not widely disseminate them to equipment operators, technicians and junior engineers, as Micron appeared to do so here.

In general, ATS 1 represents the entirety of Micron's DRAM manufacturing technology as reflected in the specific documents ATS 2-8 and identified in the United States's Bill of Particulars (*See* Dkt. 203.) Most of the information in ATS 1 is readily ascertainable by reverse engineering and is already well known in the industry. In addition, significant information about DRAM chip designs and testing/repair algorithms are missing from ATS 1 and therefore the information is incomplete for manufacturing Micron's DRAM products and implementing a successful DRAM manufacturing operation.

In general, ATS 2, ATS 6, ATS 7, and ATS 8 are the documents containing Micron DRAM Series 90 25nm Process Traveler - V90B, Micron DRAM Series 20nm Process Traveler - V00H,

Micron DRAM Series 110 1Xnm Process Traveler - Z11A, and Micron DRAM SEries 110 1Xnm Summary Process Flow based on Z11A. Most of the information in ATS 2, ATS 6, ATS 7, and ATS 8 is readily ascertainable by reverse engineering and were already well known as of late 2015 or early 2016. As much as the remaining aspects of ATS 2, ATS 6, ATS 7, and ATS 8 are focused on the specifics in each process steps, those recipes are highly specific to Micron and not easily transferred; in addition most of the process steps are in fact missing important specific parameters. In addition, significant information about DRAM chip designs and testing/repair algorithms are missing and therefore the information is incomplete for implementing a successful DRAM manufacturing operation even if another entity were to have exactly the same manufacturing equipment as Micron. These documents seem to be related to training technicians, operators, and junior engineers.

In general ATS 3 and ATS 4 are documents relating to the Implant Conditions Table for the 25nm Process. In addition, these implant conditions are so highly specific that they are only suitable for specific Micron DRAM chip designs. In fact, different Micron DRAM chips require different implant conditions. It is highly unlikely that applying these ion implant conditions on any other DRAM design would result in a functioning DRAM chip.

In general ATS 5 is the document containing Design Rules - 25nmS which are for DRAM peripheral circuitry and structures and are not related to the DRAM cell structure. Most of the information in ATS 5 is readily ascertainable by reverse engineering as evidenced by TechInsights reports and even by Micron's own reverse engineering efforts. In addition, design rules are closely tied to a specific process, and knowledge of design rules for one process has no practical value in developing a different process that requires different spacings and feature sizes.

B. The Information Contained In The Documents That The Government Has Identified As Alleged Trade Secrets 1 Through 8 Would Not Provide Independent Economic Value To UMC or Jinhua Because They Were Pursuing An Independent DRAM Design.

Professor Yang will testify that, to the extent any of the specific details in ATS 1-8 were not generally known or readily ascertainable, the government did not identify such specific details in either its Indictment (Dkt. 1) or its Bill of Particulars (Dkt. 203). The government's Bill of Particulars lists many documents, many of which are not even marked confidential. The government also identifies sections of the documents that refer to general concepts and techniques, which were already well known in the industry. The specific details provided in the government's Bill of Particulars would not have been relevant or helpful to UMC, however, since the records demonstrate that UMC had decided to pursue a different DRAM path in late 2015 or early 2016. Finally, the documents and specific details included in the Bill of Particulars provided little if any independent economic value from being maintained in secrecy.

The details of those documents were highly specific to Micron's manufacturing process and manufacturing equipment to produce their specific DRAM products. In the relevant time frame, however, it appears that UMC was pursuing a different DRAM cell structure in a different DRAM chip design and using different manufacturing equipment configurations. Internal UMC engineering documents appear to show that, sometime between December 2015 and January 19, 2016, UMC decided to pursue a 3x2 DRAM cell layout scheme that was substantially different

from Rexchip's and Micron's 25nm DRAM cell. Therefore, the details about Rexchip/Micron's process flows and cell structure would not have conferred any significant independent economic value or competitive advantage on UMC's technical development of DRAM technology. Further, DRAM cell structures cannot be trade secrets since they are readily ascertainable through reverse engineering.

Professor Yang will testify that the operation of a semiconductor manufacturing tool generally requires a "recipe" composed of hundreds or thousands of steps. Each step is defined by numerous operating parameters such as temperature, pressure, gas flow, power, voltage, etc. Changing one step within the recipe will typically affect the parameters of other steps. Due to their different structure and operation, semiconductor manufacturing tools from different suppliers require different recipes, even when they are designed to perform equivalent processes. As such, knowing the detailed recipe for an Applied Materials tool, for example, would provide limited value in developing a recipe for a Tokyo Electron tool performing an equivalent process. Moreover, the fine-tuning of a recipe depends on other processes that take place before and after the process that is being performed. As such, even where the same tool is used to perform the same process, the recipe may be different because the starting point (*e.g.*, surface preparation, layer thicknesses) is different, or because subsequent processes have different requirements.

Professor Yang will testify that UMC's DRAM design differs from Micron's in at least three ways that would render knowledge of Micron's processing steps of little or no value to UMC: (1) different physical structure of the DRAM cell and array; (2) different configuration of the manufacturing tools; and (3) different circuit design for the DRAM array and periphery.

With respect to the physical structure of the DRAM cell and array, UMC's design was entirely different from Micron's. As explained in detail below, UMC adopted a 3x2 cell design for its 25nm DRAM array, which is structurally different from Micron's 2x3 cell design in many respects, including feature widths and spacings, layer thicknesses, required aspect ratios for etch processes, etc. Accordingly, to the extent any of the details of Micron's 25nm DRAM design and manufacturing process were not generally known or readily ascertainable, they would have been inapplicable to UMC's DRAM design.

With respect to the configuration of manufacturing tools, UMC's fabrication line employed a set of tools different from Micron's. In combination with the differences in DRAM design, this resulted in a completely different set of recipes (*i.e.*, DRAM manufacturing process). Accordingly, to the extent any of the details of Micron's 25nm DRAM design and manufacturing process were not generally known or readily ascertainable, they would have been largely inapplicable to UMC's and Jinhua's manufacturing line.

C. Micron Does Not Appear to Have Taken Reasonable Measures to Keep the Information Contained in ATS 1- 8 Secret in All Instances.

Professor Yang may testify that based on his review of the documents in the case, there appear to be significant questions about whether Micron, and the companies it acquired, Elpida and Rexchip, took reasonable measures to maintain the "secrecy" of many of their alleged trade secrets. He may testify, for instance, that sensitive engineering or technical documents that are

alleged to be "trade secrets" should be closely held, and only shared with people on a need to know basis. Moreover, they should be marked "Confidential" or "Secret" to protect their secrecy.

Based on his review of the documents, Prof. Yang will testify that it appears that many of the alleged trade secret documents at issue here were essentially training documents that were widely shared with mid-level plant employees in Micron's fabrication plants. (*See* USD-0560710.) Moreover, several of the alleged trade secret documents are not marked "Confidential" or "Secret." Prof. Yang may testify that Rexchip's failure to mark these documents "Confidential" is an indicator that Rexchip and Micron did not consider these documents to be "confidential" or "secret," and did not take reasonable measures to preserve these documents' secrecy.

Further, Prof. Yang has been informed by counsel that MMT may have allowed its engineers to freely download "secret" or "confidential" information onto USB devices and work on sensitive projects at home. Prof. Yang will testify that these practices did not reflect reasonable measures or practices to protect the secrecy of confidential or secret engineering information. For example, in Prof. Yang's past experience, Hyundai Electronics (a/k/a/ SK Hynix) did not permit remote work on research projects which used sensitive DRAM information and therefore required his graduate students to work on company grounds and did not allow them to take or download sensitive DRAM information or even allow them to work remotely. As Prof. Yang may testify, prohibiting the use of USB devices to protect "confidential" or "secret" or "valuable" information is common sense in the industry.

D. <u>UMC's Engineering Documents Appear To Show That UMC Was Engaged In The Independent Development of a 3x2 25nm DRAM Cell Structure and DRAM Manufacturing Process That Was Significantly Different From Micron's 2x3 25nm DRAM, 2x3 20nm DRAM, and 3x2 1xnm DRAM Cell Structures and Manufacturing Processes and From ATS 1-8.</u>

Professor Yang will testify that the 3D physical structure and material composition of the final 3x2 25nm DRAM cell structure developed by UMC differs significantly from Micron's 2x3 25nm DRAM cell structure and even from any other Micron DRAM cell structures. This conclusion is based on direct analysis of UMC internal engineering reports (such as TAIWANHD-00004277 and reverse engineering analysis UMCDOJ-01193142) and comparison to ATS 1-8. The different physical structure and material composition of UMC DRAM is clear evidence that UMC did not copy Micron DRAM cell structures or ATS 1-8.

Further, step-by-step analyses of the UMC DRAM manufacturing process flow (such as TAIWANHD-00004277) also show significantly different materials and recipes are used to realize significantly different intermediate structures and final structures when compared to any Micron DRAM cell structure associated with ATS 1-8.

Since UMC was pursuing development of a different DRAM cell structure and was using different equipment, any information about Micron's DRAM manufacturing processes found in ATS 1-8 would have had limited value to UMC. It is further worth noting that internal UMC engineering development documents (such as TAIWANHD-02161408) appear to show that UMC decided to pursue a 3x2 DRAM cell layout which was distinctly different from a 2x3 DRAM cell layout at a very early stage in the development process (*i.e.*, TAIWANHD-02161408). The 3x2

DRAM cell layout can be seen to closely resemble designs widely known to be used by DRAM manufacturers other than Micron, and in particular the Korean manufacturers Samsung and Hynix. An example is Samsung's 3x2 20nm DRAM cell structure and layout which is shown in a TechInsights' reverse engineering SEM photograph identified as SI 39040 and is known to be a Samsung 20nm DRAM. The reason for UMC's choice of the 3x2 cell layout was likely its superior properties over the 2x3 cell layout, including greater density and performance. Internal UMC engineering documents (TAIWANHD-02161663 and TAIWANHD-00004277) clearly show that UMC was developing a DRAM cell structure which seems to more closely track Samsung's 20nm DRAM cell structure or Hynix 21nm DRAM cell structure, as implied by the inclusion of multiple TechInsights reverse engineering SEM images of detailed DRAM cell sub structures from both Samsung 20nm DRAM and Hynix 21nm DRAM.

Internal UMC engineering documents (*see e.g.,* UMCDOJ-00125243, "Project M Milestone V2~V3 _20160128-neillee.pptx", UMCDOJTT-00000213, UMCDOJTT-00148191 and UMCDOJTT-00000192) show independent engineering development of important DRAM cell sub structures, process recipes for critical pattern formation, performance comparisons of equipment from different suppliers, and also significant amounts of scheduled internal project development time. Furthermore, these internal documents also appear to demonstrate that UMC was able to leverage its familiarity and experience with semiconductor manufacturing which allowed it to make use of its existing equipment and internal engineering expertise (*see., e.g.,* "Project M Milestone V2~V3 _20160128-neillee.pptx" at 18-19).

Based on his review of the documents, Prof. Yang does not see any evidence that UMC copied the Rexchip/Micron DRAM manufacturing process for Micron's 2x3 25nm DRAM cell structure into the final UMC DRAM manufacturing process flow for UMC's 3x2 25nm DRAM cell structure. In fact, the documents show planning and independent engineering effort to develop a UMC DRAM manufacturing process that used different equipment while leveraging UMC's considerable semiconductor manufacturing facilities and experience. Although some of the files identified by Dr. Dyer (*see* TAIWANHD-02160180) include what appears to be Rexchip information on the "4G3D Flow (2013,0614)" DRAM manufacturing process, that Rexchip information (1) was not marked confidential by Micron on Rexchip in other documents, (2) was probably already familiar and properly known to many of the UMC engineers through their previous work experience at Elpida or Rexchip, and (3) at most, seems to have served as a temporary generic placeholder since the resulting structure and process steps employed by UMC were necessarily and materially different. The apparent conclusions of internal UMC technical meetings to use different equipment and different recipes could have been reached without the specific Rexchip information.

Further, based on Professor Yang's review of the documents, there is evidence that UMC took efforts to strip out any influence that Kenny Wang had in determining the parameters of UMC's design rules. Based on the documents Prof. Yang has reviewed, coupled with the testimony from the Taiwan trial, Professor Yang understands that Kenny Wang only provided inputs into design rule parameters for the DRAM periphery structures and circuits which were readily ascertainable from reverse engineering and/or were non-critical to the product. For example, Kenny Wang was purportedly asked to provide input into the minimum overlap required for ion implantation masks. Those ion implantation masks were used to delineate a larger area while the physical structure provided a smaller self-aligned window for the ion implantation. The

amount of overlap was non-critical and inconsequential to any semiconductor structures manufactured by UMC. To the extent Kenny Wang's inputs may have had any value to UMC, Prof. Yang will testify that the documents produced by UMC appear to reflect that UMC spent significant effort to remove those inputs from the final DRAM design rules and revise the key parameters based on independent sources.

In all, Professor Yang may testify that there is evidence to demonstrate that UMC undertook an independent DRAM design and testing process, and was not copying or relying on any Micron information found in ATS 1-8.

E. UMC's 3x2 25nm DRAM Cell Structure and Manufacturing Process Flow Were Substantially Different from Micron's 25nm DRAM and 20nm DRAM Cell Structures and Manufacturing Process Flows (ATS 1-6).

The 3D physical structure and material composition of UMC's 3x2 25nm DRAM cell structure was substantially different from both Micron's 2x3 25nm DRAM and 2x3 20nm DRAM cell structure. Most obviously, the shape of UMC's 3x2 DRAM cell layout is very different from Micron's 2x3 DRAM cell layouts. In addition, many of the DRAM substructures have different compositions and sizes. Finally, those fundamental differences in DRAM cell structure composition, shape, and sizes are clearly the result of significant differences in the manufacturing process flow. Furthermore, detailed analysis of UMC's DRAM manufacturing process flow appears to show that it is based on different manufacturing equipment than MMT, Rexchip and Elpida (*see* UMCDOJ-00919365) and contains significant differences in process recipes when compared to information in ATS 1-6. Key aspects of this opinion are further set forth in Section VI(C), above.

F. UMC's 3x2 25nm DRAM Cell Structure and Manufacturing Process Flow Was Substantially Different from Micron's 1xnm DRAM Cell Structure and Manufacturing Process Flow (ATS 7-8).

The 3D physical structure and material composition of UMC's 3x2 25nm DRAM cell structure was substantially different from Micron's 3x2 1xnm DRAM cell structure resulting from DRAM manufacturing process flows described in ATS 7-8. While the overall 3x2 DRAM cell layout used by UMC and the Micron cell layout described in ATS 7-8 share some visible similarities, which are further discussed below, there are many clear and significant differences between the two DRAM cell structures, including obvious differences in absolute DRAM cell size (e.g. 78nm x 80nm vs 61.2nm x 53nm), Capacitor Structures (*e.g.*, double lattice using a high K dielectric of ZrO/AlO/ZrO vs triple lattice using a high K dielectric of ZrOx complex – *see* UMCDOJTT00000101 and ATS 8), and more subtle differences in the sizes and shapes of DRAM cell sub structures (*e.g.*, buried wordline depth and fin size). These significant differences in DRAM cell structure and material composition were the obvious consequence of using different DRAM manufacturing process flows. Furthermore, the general concept of 3x2 DRAM cell layout pattern as used by both UMC and Micron were well known and actually implemented by Samsung 20nm DRAM well before 2014. In addition, the use of lattice support structures and high K dielectrics for DRAM capacitors was also very well known in the industry.

DRAM cell structures used by Samsung, Hynix, and Micron all shared many similarities. In fact, all DRAM cell structures used by these companies were based on 6F2 cell with open bit line architecture, used a buried wordline with a metal bitline above the wordline, and finally incorporated a storage capacitor stacked on top. These structures were well known and readily ascertainable through reverse engineering (*see e.g.*, TechInsights Hynix 21nm DRAM UMCDOJTT-00028770, TechInsights Samsung 20nm DRAM UMCDOJTT-00029513, Micron competitor analysis USD-0001493 and USD-0001641. Furthermore, the general process sequence of first forming Shallow Trench Isolation for Active Areas followed by buried Wordlines and Bitlines, and subsequently followed by forming of Storage Capacitors was readily deduced and well known in the industry. Finally, the overall process sequence and general concepts were well known to engineers and technicians with experience developing DRAM including many UMC engineers.

G. Professor Yang Disagrees with the Allegations in the Indictment that the Disclosures and Inventions Described in UMC and Jinhua's Joint Patents and Patent Applications Were Based On or Derived from Any Alleged Proprietary or Secret Micron Materials Identified in ATS 2 and 6.

The Indictment alleges that certain patents and patent applications purportedly jointly filed by UMC and Jinhua contained "disclosures and inventions" that were "based on or derived from misappropriated proprietary Micron materials identified in Trade Secrets 2 and 6" and that this alleged information "could not be obtained through reverse engineering." (*See* Dkt. 1, ¶¶ 32, 45.) The government has not identified any independent experts or Micron lay experts who will testify on this issue, so it appears that the government will not be advancing that argument at trial and has waived the ability to do so by not making a timely disclosure under Rule 16 of its intent to do so. In the event that the government were to present any testimony or other evidence on this issue, however, Prof. Yang would explain why the government's allegations are unfounded.

H. The Proposed Timeline For The Development Of DRAM Technology Set Forth In UMC And Jinhua's Technology Cooperation Agreement Was Reasonable.

Professor Yang will testify that he has reviewed the Technology Cooperation Agreement ("TCA") between UMC and Jinhua, dated May 13, 2016, and that he understands that the TCA provided for UMC to develop two new DRAM nodes, titled 32nm and 32Snm, over an approximately four year period form May 2016 through the fourth quarter of 2020. Prof. Yang will testify that based on his understanding of the technology and UMC's capabilities, this seemed like a feasible engineering task given UMC's significant resources and considerable experience in semiconductor manufacturing, including manufacturing of DRAM products. In early 2016, the overall Project M schedule was to attempt pilot mass manufacturing of UMC DRAM at Fujian around Q2/Q3 2018 with an unspecified amount of time for achieving successful mass production yields (*see e.g.*, TAIWANHD-02161629; "Project M Milestone V2~V3 _20160128-neillee.pptx"). This also included significant Research and Development effort by UMC until the end of 2016. This was over 2 years of development time before the first attempt at pilot mass production at Jinhua which is significantly longer than might be expected for a simple technology transfer. In addition, by proper selection of 3x2 DRAM cell layout, UMC Project M could clearly benefit from the proven 20nm and 21nm DRAM products of Samsung and SK Hynix. Prof. Yang will testify that he believes this timeline was commercially reasonable given that UMC had

significant resources and experience in advanced semiconductor manufacturing and in the electronics industry and strong business relationships with major semiconductor equipment manufacturers, highly capable design houses, electrical test subcontractors, and packaging subcontractors.

I. Based On Professor Yang's Review Of UMC Documents, He Does Not See Any Evidence That Jinhua Played An Active Role In UMC's Research And Development Or Design Of Its DRAM Technology.

Professor Yang may testify that, in his review of UMC documents, he has seen no evidence that Jinhua played an active role in UMC's Research and Development ("R&D") or design of its DRAM technology that was later transferred to Jinhua. Based on the evidence Prof. Yang has seen, Jinhua's role during the design process was primarily non-technical (*i.e.*, to check in with UMC on UMC's progress in design development and to coordinate the purchase of machines for manufacturing and start employee recruitment). (*See, e.g.,* TAIWANHD-00000467; USD-0667686; USD-0669206; TAIWANHD-02161623.) Moreover, many of the documents transferred from UMC to Jinhua were educational or training materials at a very basic and fundamental level. (*See, e.g.* TAIWANHD-02161623.) As a result, Prof. Yang may testify that Jinhua does not appear to have been involved in the technical aspects of DRAM development under the Technology Cooperation Agreement, and that Jinhua's role under the Agreement was primarily to make sure it purchased the correct equipment and established suitable facilities needed for the manufacturing end of the Technology Cooperation Agreement (*see* D-0000658). In fact, Prof. Yang may testify that the only evidence he has seen of Jinhua's involvement in the Technology Cooperation Agreement was in making sure that Jinhua built an industry-standard fabrication facility (essentially, just a "shell" for the manufacturing tools) and bought and installed the necessary equipment required for the fabrication plants in Mainland China. (*Id*.)

Finally, Professor Yang may testify that he has not seen anything in the UMC technology itself that would have put Jinhua on notice of any use by UMC of Micron's proprietary technology. On the contrary, the fact that UMC took a different approach to DRAM design from Micron (*e.g.*, the 3x2 DRAM cell layout instead of the 2x3 DRAM cell layout then employed by Micron) would have indicated to Jinhua that UMC's technology was significantly different from and unrelated to Micron's.

J. Professor Yang's Responses to Opinions by Dr. Dyer and Mr. Daly.

To the extent that the opinions summarized above do not already address all of Dr. Dyer's and Mr. Daly's opinions, Prof. Yang may also offer the following opinions:

1. Professor Yang's Response to Dr. Dyer's Opinion That UMC "Appropriat[ed]" Micron's Process.

While the Rexchip 4G3D process flow was inserted into the document that Dyer refers to as the "Meeting minutes" (TAIWANHD-02160180) from December 2015, Professor Yang will testify that the general sequence of that process flow was already well known to highly skilled UMC engineers such as JT Ho. Professor Yang will testify that, at most, the technical notes from the December 2015 "Meeting minutes" appear to show that the author of that document was

considering using different semiconductor manufacturing equipment and therefore a different process flow would need to be developed with certain critical areas involving greater technical risk and effort. Essentially these same conclusions would likely have been reached by highly skilled UMC engineers such as JT Ho without the 4G3D information. The Project M process flow in TAIWANHD-0216192 simply shows that groups of process steps were renamed according to their well-known overall function (*i.e.,* STI AA and PWELL) and seems to have been last modified on December 18, 2015.

Approximately one month later, internal UMC documents indicate that UMC Project M had selected to pursue development of a 3x2 DRAM cell layout based on file metadata indicating the last modified date of January 11, 2016. Furthermore, a subsequent early draft of the Project M process flow in TAIWANHD-02161367 which seems to have been last modified on February 19, 2016, showed significant differences from ATS 1-8, since UMC was pursuing a 3x2 DRAM cell layout and needed a significantly different DRAM manufacturing process from the Rexchip 4G3D process flow. By February 19, 2016, Project M was apparently already significantly different from any Micron design. These were significant changes and were well beyond anything that would be normally expected when just transferring semiconductor manufacturing technology to a new facility. Transferring semiconductor manufacturing technology required careful matching of semiconductor manufacturing equipment. This can be clearly seen in TAIWANHD-00032607 and TAIWANHD-00032608 where Micron was very careful in selecting its semiconductor manufacturing equipment to better facilitate smooth technology transfer and looking to actively minimize technical risks due to differences in equipment between their own manufacturing facilities. By February 2016, the Project M process flow showed critical process steps that seem to have been based on UMC's own experience and knowledge and were significantly different from information in ATS 1-8 and were even significantly different from UMC's final technology transfer package delivered in Sept 2018. This appears to indicate that UMC was engaged in independent research and development of a 3x2 25nm DRAM manufacturing process.

Since the same well known overall sequence of general processing steps is used to make well known DRAM structures, it is not surprising that side-by-side flow comparisons (such as Dr. Dyer's Exhibit 5) may be superficially similar. However, detailed comparisons of the recipes show different equipment using different processing parameters that necessarily result in different DRAM structures. In fact, the buried wordlines and storage capacitors of all 6F2 DRAM cells from different companies share superficial similarities (*see, e.g.,* USD-0001493 and USD-0001641, which show Micron reverse engineering and the similarity of Samsung's and Hynix's structures to Micron's). However, UMC's and Micron's DRAM cell structures are distinctly different and were manufactured using distinctly different processes on different types of semiconductor manufacturing equipment. The similarity is simply a consequence of the industry following proven and well known manufacturing methods.

Finally, the general sequences of processing steps can be readily deduced from a basic understanding of the capabilities of semiconductor manufacturing equipment and reverse engineering analysis of the semiconductor structures.

2. Professor Yang's Response to Mr. Daly and Dr. Dyer's Suggestions that UMC's Timetable was Overly Aggressive and Not Feasible For Independent Development.

Prof. Yang will testify, as discussed above, that he believes that the development timetable set forth in the Technology Cooperation Agreement was reasonable under the circumstances and he disagrees with Mr. Daly's opinion that it was only consistent with "the adoption of DRAM technology from a third party." (*See* Daly Report at 2.) Among other reasons, this is because developing a "trailing edge" technology like UMC and Jinhua were trying to develop in this case was significantly easier than being the first to develop "leading edge" technology. The issue of technical feasibility was no longer in question and by legitimate reverse engineering, it is possible to find a successful development path and many technical dead ends could be avoided. Furthermore, significant cost and time advantages can be properly saved by reverse engineering and by the fact that many techniques, materials, and equipment have already been developed and are available for analysis and purchase.

By legitimately surveying the DRAM industry, UMC was able to appropriately and correctly determine that the 3x2 DRAM cell structure was superior. In fact, the superiority of the 3x2 DRAM cell structure was already well known in the industry as evidenced by the Samsung 20nm DRAM and Hynix 21nm DRAM, which UMC Project M had studied and carefully analyzed. In addition, by starting from a "green field" (*i.e.*, tabula rasa), UMC did not have to be concerned about previously sunk investments in less appropriate (*i.e.*, legacy) semiconductor manufacturing equipment and in preserving compatibility with previous generations of DRAM manufacturing technology.

Professor Yang will also testify that UMC had significant resources and experience in advanced semiconductor manufacturing and in the electronics industry, including DRAM manufacturing. It already possessed and managed state-of-the-art clean room facilities for semiconductor manufacturing of 200mm and 300mm silicon wafers. UMC already had strong business relationships with all of the major semiconductor equipment suppliers. UMC also had relationships with many highly capable design houses, electrical test sub-contractors, and packaging subcontractors. (*See* UMCDOJ-00139087; UMCDOJ-00172570; UMCDOJ-01040964.)

Considering the legitimate advantages of UMC's Project M, the overall project structure and schedule was reasonable. In early 2016, the overall Project M schedule was to attempt pilot mass manufacturing of UMC DRAM at Fujian around Q2/Q3 2018 with an unspecified amount of time for achieving successful mass production yields (*see* TAIWANHD-02161629; "Project M Milestone V2~V3 _20160128-neillee.pptx"). This also included significant Research and Development effort by UMC until the end of 2016. This was over 2 years of development time before the first attempt at pilot mass production which is significantly longer than might be expected for a simple technology transfer. In addition, by proper selection of 3x2 DRAM cell layout, UMC Project M could clearly benefit from the proven 20nm and 21nm DRAM products of Samsung and SK Hynix to rapidly follow more advanced 20nm and 1xnm DRAM technology.

3. Professor Yang's Response to Dr. Dyer's Opinions Regarding the Reasons He Believes that UMC Decided to Obtain Design Drawings from UMI.

Professor Yang will testify that the collaboration and interaction between UMC Project M and UMI was essentially focused on the DRAM periphery circuitry and electrical performance of the periphery transistors and not the DRAM cell structure and was focused on tuning the

performance of DRAM peripheral circuitry to match UMC's different DRAM cell array characteristics.

Detailed design information and electrical characteristics of DRAM cell array structure and DRAM peripheral circuitry are readily ascertainable by reverse engineering (*see* USD-0001493; USD-0001641; TAIWANHD-00000691). Every DRAM manufacturer uses essentially the same well known and well proven circuitry for DRAM peripheral circuitry. The electrical characteristics of UMC's DRAM cell structure and array were significantly different from Micron's 25nm DRAM (*see* TAIWANHD-02161663). Therefore, simply using the exact same design of DRAM peripheral circuitry from Micron or any other DRAM manufacturer would be highly unlikely to work and would be far from optimal. UMC appears to have provided estimated nominal electrical characteristics of their devices to UMI (*see* "Transitror%20dimention%20trend%20for%20DRAM%20development((Autosaved-30569233157692639 3)).ppt") which subsequently tuned and optimized DRAM peripheral circuitry to match the electrical characteristics of UMC's DRAM array to ensure functionality and high yield. There seemed to have been many subsequent technical meetings between UMC and UMI to discuss these optimizations. These are very normal and common technical meetings that might occur between a DRAM foundry (*i.e.*, UMC) and DRAM design house (*i.e.*, UMI). UMC's DRAM array was clearly not a copy of Micron's 25nm DRAM array. UMC and UMI appear to have developed an optimized design for DRAM peripheral circuitry to match UMC's DRAM array.

Professor Yang will testify that it is well known that the performance of the periphery transistors needs to be optimized depending on the performance of the DRAM cell and the desired DRAM product specifications. DRAM periphery transistors are comparatively very simple planar CMOS transistors and have the same basic structure as older generation Logic semiconductor products of which UMC has a great deal of resources, experience, and knowledge. Adjusting and optimizing DRAM periphery transistor performance with ion implantation and transistor structure optimization would be a routine and typical activity well within the expertise of UMC engineers.

The appropriate sequence and dose/energy of ion implants for CMOS transistors are well known in the industry (*e.g.*, lightly doped drain (LDD) implants are performed the formation of sidewall spacers while source/drain (S/D) implants are usually higher dose and are performed after the formation of sidewall spacers on the transistor gate, while lightly doped drain implants are performed the formation of sidewall spacers). Therefore, Prof. Yang will testify that any apparent similarities between UMC Project M and Micron DRAM processes are simply the result of the industry following well known concepts and common techniques.

EXHIBIT 1

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Education:

Massachusetts Institute of Technology — August 1990
Ph.D. in Electrical Engineering and Computer Science
Thesis: ``The Architecture and Design of CCD Processors for Computer Vision''

Massachusetts Institute of Technology — January 1987
S.M. in Electrical Engineering and Computer Science
Thesis: ``Low Pressure Nitrided Oxide in MOS Capacitors''

University of California, Berkeley — May 1984
B.S. in Electrical Engineering and Computer Science

Research and Professional Experience:

Professor of Electrical Engineering and Computer Science
School of Engineering and Applied Sciences, Harvard University
- Gordon McKay Professor — September 1997 - present
- Associate Professor — September 1994 - 1997
- Assistant Professor — September 1990 - 1994

Analysis, design and implementation of microelectronic circuits and VLSI systems.
Teaching and curriculum planning in electrical engineering and computer science.

Founder and Program Director — September 2015 - present
Master in Design Engineering at Harvard University
Collaborative 2-year degree program at Harvard Graduate School of Design and School of Engineering and Applied Sciences

HBS University Fellow and Visiting Professor — September 2008 – May 2012
Harvard Business School
Research and teaching in disruptive innovation, technology transfer, and industry evolution.

Founder and CEO — March 2000 – March 2008
Silicon7, Incorporated
Seongnam-si, Kyoungki-do, KOREA
Application Specific Memory products for mobile communications and computing platforms.

Science and Technology Board Member — June 1998 – June 2001
Polaroid Corporation, Cambridge, Massachusetts
Evaluation of research and technology developments.

Consultant and Senior Fellow — August 1995 – March 2000
Hyundai Electronics Industries, Ichon, Korea
Development of high performance CMOS image sensor technology for embedded image sensing and processing applications. Research on advanced DRAM design and merged memory logic (MML) technology for advanced computer systems.

Consultant — December 1993 - June 1998
Hamamatsu Photonics K.K., Hamamatsu City, Japan
Development of smart image sensors and CCD/CMOS analog charge-domain circuitry.

Consultant — June 1991 - December 1993
Istituto per la Ricerca Scientifica e Tecnologica (IRST), Trento, Italy
Research and development of advanced CMOS/CCD technology and circuitry.

Consultant — June 1988 - August 1990
M.I.T. Lincoln Laboratory, Dr. Alice M. Chiang, Advisor
Design and implementation of CCD image sensors and analog signal processors.

Research Assistant — September 1987 - August 1990
M.I.T. Artificial Intelligence Laboratory, Professor Tomaso Poggio, Advisor
Implementation of analog VLSI hardware for computer vision.

Research Assistant — September 1984 - August 1987
M.I.T. Microsystems Technology Laboratory, Professor Charles G. Sodini, Advisor
Development and characterization of low pressure ammonia and oxygen annealing process for improved reliability of scaled MOS transistors.

Research Assistant — January 1983 - May 1984
U.C. Berkeley Electronic Research Laboratory, Professor Chenming Hu, Advisor
Measurement and analysis of hot electron degradation in MOS transistors.

Honors and Awards:

National Science Foundation Young Investigator Award	1992
Army Research Office Young Investigator Award	1992
Hertz Foundation Fellowship	1984 – 1990
National Science Foundation Fellowship	1984
University of California Alumni Scholarship	1980 - 1984
Phi Beta Kappa, Eta Kappa Nu, Tau Beta Pi	1984

Patents:

Method and Charge--Coupled Apparatus for Algorithmic Computations, Woodward Yang, May 12, 1992, U.S. Patent No. 5,113,365.

Image Sensor Array With Threshold Voltage Detectors and Charged Storage Capacitors, Woodward Yang, May 25, 1993, U.S. Patent No. 5,214,274.

Error Correcting Sigma-Delta Modulation Decoding, Philip Steiner and Woodward Yang, November 17, 1998, U.S. Patent No. 5,838,272.

CMOS image sensor with equivalent potential diode, Woodward Yang, Ju Il Lee and Nan Yi Lee, February 26, 1999, US Patent No. 6,180,969.

CMOS image sensor with equivalent potential diode and method for fabricating the same, Woodward Yang, Ju Il Lee and Nan Yi Lee, February 26, 1999, US Patent No. 6,184,055.

CMOS image sensor with testing circuit for verifying operation thereof, Oh Bong Kwon, Woodward Yang, Suk Joong Lee, and Gyu Tae Hwang, February 26, 1999, US Patent No. 6,633,335.

Antifuse circuitry for post-package DRAM repair, Woodward Yang, et al., January 10, 2000, US Patent No. 6,240,033.

Image sensor with analog-to-digital converter that generates a variable slope ramp signal, Kang Jin Lee, Chan Ki Kim, Jae Won Eom and Woodward Yang, February 8, 2001, US Patent No. 6,545,624.

Error-correcting circuit for high density memory, Elaine Ou and Woodward Yang, June 9, 2009, US Patent No. 7,546,517.

Selected Presentations, Interviews and Invited Lectures:

“Chip Industry must learn not to overshoot,” EE Times cover page, interview and commentary, June 6, 2006.

“Disruptive Innovation,” Keynote Speaker at Consumer Electronics Show, January 2006.

“Using DRAM Technology to Make SRAM,” The Weekly Economist interview, September 24, 2002.

“Silicon7 8-Mbit SRAM sports single-transistor cell,” EE Times interview, September 2001.

“Hyundai modifies DRAM process to produce CMOS image sensors,” EE Times interview, March 1999.

“Merged Memory Logic,'' W. Yang, IEEE Solid-State Circuits Society Distinguished Lecturer, Hanyang University, Korea, March 1999.

``The Dawn of Billion Transistor Chips,'' W. Yang, 1998 Korea - U.S. Science and Technology Symposium: Computing and Telecommunication, Chicago, April 1998.

``Innovation in Microelectronic Manufacturing,'' W. Yang, National Research Council Workshop on the Electronics Industry, November 1997.

``Trends in Electronic Image Sensing and Processing,'' IEEE Laser and Electro Optical Society, Lincoln, MA, March 1996.

Selected Depositions and Trial Testimonies:

In the matter of CERTAIN ELECTRONIC DEVICES, INCLUDING MOBILE PHONES, PORTABLE MUSIC PLAYERS, AND COMPUTERS (ITC, Investigation No. 337-TA-701, deposition and trial) – retained by Nokia

In the matter of APPLE, INC. vs. SAMSUNG ELECTRONICS COMPANY, LTD. (United State District Court, Northern District of California, Civil Action No. 11-CV-01846-LHK, deposition and trial) – retained by Samsung

In the matter of CERTAIN CONSUMER ELECTRONICS WITH DISPLAY AND PROCESSING CAPABILITIES, (ITC, Investigation No. 337-TA-885, deposition and trial) – retained by Toshiba

In the matter of CERTAIN GRAPHICS PROCESSING CHIPS, SYSTEMS ON A CHIP, AND THE PRODUCTS CONTAINING THE SAME, (ITC, Investigation No. 337-TA-941, deposition and trial) – retained by NVidia

In the matter of US Patent 6,418,310 (US Patent and Trademark Office, Patent Trial and Appeal Board, IPR2015-05183, deposition) – retained by Ericsson Inc.

Publications:

“Cambridge NanoTech,” Woodward Yang and David Kiron, Harvard Business School Case Study 9-610-083, Boston, MA, Harvard Business School, May 2010.

"Science and Technology Entrepreneurship for Greater Societal Benefit: Ideas for Curricular Innovation," Fleming, Lee, Woodward Yang, and John Golden in **Spanning Boundaries and Disciplines: University Technology Commercialization in the Information Age**, edited by Gary D. Libecap, Marie Thursby and Sherry Hoskinson, Emerald Group Publishing Limited, 2010.

"The New Economics of Semiconductor Manufacturing," Clayton Christensen, Steve King, Matt Verlinden and Woodward Yang, **IEEE Spectrum**, vol. 45, issue 5, pp. 24-29 May 2008.

"Energy Consumption Model for Power Management in Wireless Sensor Networks," Qin Wang and Woodward Yang, *IEEE Communications Society Conference on Sensor, Mesh and Ad Hoc Communications and Networks SECON 2007*, June 2007.

"A Realistic Power Consumption Model for Wireless Sensor Network Devices," Qin Wang, Mark Hempstead and Woodward Yang, *IEEE Communications Society Conference on Sensor, Mesh and Ad Hoc Communications and Networks SECON 2006*, September 2006.

"Fast Error-Correcting Circuits for Fault-Tolerant Memory," E. Ou and W. Yang, *IEEE International Workshop on Memory Technology, Design and Testing*, pp. 8-12, August 2004.

"A Low-Power 256-Mb SDRAM with an On-Chip Thermometer and Biased Reference Line Sensing Scheme," J.P. Kim, W. Yang, and H.-Y. Tan, **IEEE Journal of Solid-State Circuits**, vol. 38, no. 2, pp. 329-337, February 2003.

"An Antifuse EPROM Circuitry Scheme for Field-Programmable Repair in DRAM," J.K. Wee, W. Yang, E.K. Ryou, J.S. Choi, S.H. Ahn, J.Y. Chung and S.C. Kim, **IEEE Journal of Solid-State Circuits**, vol. 35, no. 10, pp. 1408-1414, October 2000.

"An Embeddable Low Power SIMD Processor Bank," S.-H. Hong and W. Yang, *Digest of Technical Papers of IEEE International Solid-State Circuits Conference*, pp. 192-193, February 2000.

"Antifuse EPROM Circuit for Field Programmable DRAM," J.-S. Choi, J.-K. Wee, P.-J. Kim, J.-K. Oh, C.-H. Lee, H.-Y. Cho, J.-Y. Chung, S.-C. Kim and W. Yang, *Digest of Technical Papers of IEEE International Solid--State Circuits Conference*, pp. 406-407, February 2000.

"A Novel Double Slope Analog-to-Digital Converter for a High-Quality 640 x 480 CMOS Imaging System," O.-B. Kwon, K.-N. Park, D.-Y. Lee, K.-J. Lee, S.-C. Jun, C.-K. Kim, and W. Yang, *6th International Conference on VLSI and CAD 1999*, pp. 335-338, Seoul, Korea, October 1999.

"An Improved Digital CMOS Imager," O.-B. Kwon, K.-N. Park, D.-Y. Lee, K.-J. Lee, S.-C. Jun, C.-K. Kim, Y.-B. Lee and W. Yang*, IEEE Workshop on Charged-Coupled Devices and Advanced Image Sensors*, Nagano, Japan, June 1999.

"A Linear-Response, High-Dynamic Range CMOS Imager Suitable for Spectroscopic Applications," D. Qian and W. Yang, *IEEE Workshop on Charged-Coupled Devices and Advanced Image Sensors*, Nagano, Japan, June 1999.

"New Self Refresh Scheme Using Cell Leakage Monitoring Circuit," Y.-H. Seol, H.-Y. Cho, J.-K. Wee, D.-H. Ryu, J.-G. Oh, J.-S. Choi, J.-J. Lee, J.-H. Lee, and W. Yang, (in Korean) *Proceedings of the 6th Korean Conference on Semiconductors*, pp. 377-378, Seoul, Korea, February 1999.

"High Voltage Circuitry for Post Package DRAM Repair," P.-J. Kim, J.-G. Oh, J.-K. Wee, D.-H. Ryu, Y.-H. Seol, H.-Y. Cho, J.-S. Choi, J.-H. Han, J.-H. Lee, and W. Yang, (in Korean) *Proceedings of the 6th Korean Conference on Semiconductors*, pp. 385-386, Seoul, Korea, February 1999.

``An Integrated 800 x 600 CMOS Imaging System,'' W. Yang, O.-B. Kwon, J.-I. Lee, G.-T. Hwang and S.-J. Lee, *Digest of Technical Papers of IEEE International Solid--State Circuits Conference*, pp. 304-305, February 1999.

``VLSI Hardware for Example-Based Learning,'' A. Lipman and W. Yang, **IEEE Transactions on VLSI Systems**, vol. 5, no. 3, pp. 320-328, September 1997.

``A Reconfigurable VLSI Coprocessing System for the Block Matching Algorithm,'' A. Bugeja and W. Yang, **IEEE Transactions on VLSI Systems**, vol. 5, no. 3, pp. 329-337, September 1997.

``A CCD/CMOS Image Sensor Array with Integrated A/D Conversion,'' M. Gottardi and W. Yang, *Proceedings of the IEEE International Symposium on Circuits and Systems*, Vol. III, pp. 1908-1911, June 1997.

``Circuit integration pushes image sensor performance,'' W. Yang, **Laser Focus World**, Penwell Publishing, pp. 129-139, February 1997.

``A Framework for Analysis of High Order Sigma-Delta Modulators,'' P. Steiner and W. Yang, **IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing**, vol. 44, no. 1, pp. 1-12, January 1997.

``Competitive learning algorithms for channel optimized vector quantizers,'' D. Martinez and W. Yang, *The 1996 IEEE International Conference on Neural Networks*, pp. 1462-1467, June 1996.

``Stability of High Order Sigma-Delta Modulators,'' P. Steiner and W. Yang, *Proceedings of IEEE International Symposium on Circuits and Systems*, Vol. III, pp. 52-57, May 1996.

``Simple Pulse Asynchronous State Machines,'' J. Miller and W. Yang, *Proceedings of IEEE International Symposium on Circuits and Systems*, Vol. III, pp. 405-409, May 1996.

``Neuromorphic CMOS Circuitry for Active Bidirectional Delay Lines,'' W. Yang, *Proceedings of IEEE International Symposium on Circuits and Systems*, Vol. III, pp. 473-476, May 1996.

``A Robust Backward Adaptive Quantizer,'' D. Martinez and W. Yang, *Proceedings of IEEE Workshop on Neural Networks for Signal Processing V*, pp. 531-540, August 1995.

``A Real-Time Face Recognition System Using Machine Vision Techniques,'' W. Yang, invited paper, *CardTech/SecurTech Conference Proceedings*, pp. 179-193, April 1995.

``Stability Analysis of the Second Order Sigma-Delta Modulator,'' P. Steiner and W. Yang, *Proceedings of IEEE International Symposium on Circuits and Systems*, Vol. V, pp. 365-368, June 1994.

``An Interline CCD Imaging Array with On-Chip A/D Conversion,'' D. J. Friedman and W. Yang, *Proceedings of SPIE, Charge--Coupled Devices and Solid State Optical Sensors IV*, vol. 2172, pp. 54-63, February 1994.

``A Wide Dynamic Range, Low Power Photosensor Array,'' W. Yang, *Digest of Technical Papers of IEEE International Solid--State Circuits Conference*, pp. 230-231, February 1994.

``A Real--Time Face Recognition System Using Custom VLSI Hardware,'' J.M. Gilbert and W. Yang, *Proceedings of IEEE Workshop on Computer Architectures for Machine Perception*, pp. 58-66, December 1993.

``A CCD/CMOS Image Motion Sensor,'' M. Gottardi and W. Yang, *Digest of Technical Papers of IEEE International Solid—State Circuits Conference*, pp. 194-195, February 1993.

``Analog CCD Processors for Image Filtering,'' W. Yang, *Proceedings of SPIE, Visual Information Processing: From Neurons to Chips*, vol. 1473, pp. 114-127, April 1991.

``The MIT Vision Chip Project: Analog VLSI Systems for Fast Image Acquisition and Early Vision Processing,'' J.L. Wyatt, D.L. Standley, and W. Yang, *Proceedings of the International Conference on Robotics and Automation*, vol. 2, pp. 1330-1335, April 1991.

``A Full Fill--Factor CCD Imager with Integrated Signal Processors,'' W. Yang and A.M. Chiang, *Digest of Technical Papers of International Solid--State Circuits Conference*, pp. 218-219, February 1990.

``A Charge--Coupled Device Architecture for On Focal Plane Image Signal Processing,'' W. Yang, *Proceedings of International Symposium on VLSI Technology, Systems, and Applications*, pp. 266-270, May 1989.
``Optical Flow: Computational Properties and Networks, Biological and Analog,'' Tomaso Poggio, Woodward Yang, and Vincent Torre, **The Computing Neuron**, R. Durbin, C. Maill, and G. Mitchison (editors), pp. 255-370, Addison--Wesley, New York, 1989.

``Optimization of Low Pressure Nitridation/Oxidation of SiO_2 for Scaled MOS Devices,'' W. Yang, R. Jayaraman, and C.G. Sodini**, IEEE Transactions on Electron Devices**, vol. ED-35, no. 7, pp. 935-944, July 1988.

``Radiation Effects in Low Pressure Reoxidized Nitrided Oxide Gate Dielectrics,'' G. Dunn, R. Jayaraman, W. Yang, and C.G. Sodini, **Applied Physics Letters**, vol. 52, no. 20, pp 1713-1715, May 1988.

``The MIT Vision Machine,'' T. Poggio, J. Little, E. Gamble, W. Gillet, D. Geiger, D. Weinshall, M. Villalba, N. Larson, T. Cass, H. Bulthoff, M. Drumheller, P. Oppenheimer, W. Yang, and A. Hurlbert, *DARPA Image Understanding Workshop*, pp. 177-198, April 1988.

``MOS Electrical Characteristics of Low Pressure Re—oxidized Nitrided Oxide,'' R. Jayaraman, W. Yang, and C.G. Sodini, *Technical Digest of International Electron Devices Conference*, pp. 668-671, December 1986.

``Hot Carriers Induced Degradation in Thin Gate Oxide MOSFET's,'' M--S. Liang, C. Chang, W. Yang, C. Hu, and R.W. Brodersen, *Technical Digest of International Electron Devices Conference*, pp. 186-189, December 1983.

Additional Patent Consulting Work between 2012 to present (not mentioned in CV)
Woodward Yang (as of January 2019)

In the matter of Imperium Holdings, Inc. v Apple, Kyocera Communication, Inc., LG Electronics, USA, Inc, LG Electronics Mobilecomm, USA, Inc, Motorola Mobilecomm USA, Motorola Mobility, Inc., Nokia Inc, Research in Motion Corporation, and Sony Ericsson Mobile Communications (USA), Inc., (United States District Court, Eastern District of Texas, Sherman Division, Case No. 4:11-cv-163-RC-ALM, deposition) – retained by Nokia

In a confidential matter (2013-2015) related to four patents related to semiconductor image sensors
6,023,081 Semiconductor Image Sensor
6,221,686 Method of making a semiconductor image sensor
6,979,587 Image sensor and method for fabricating the same
7,365,298 Image sensor and method for manufacturing the same

In a matter of Radiancy, Inc., v. Viatek Consumer Products Group, Inc. (United States District Court, Southern District of New York, Case No. 13 Civ. 3767-NSR-LMS, deposition) – retained by Radiancy

In a confidential matter (2016) related to two patents for an automobile manufacturer
6,339,428 Method and Apparatus for Compressed Texture Caching in a Video Graphics System
7,254,721 System and Method for Controlling an Integrated Circuit to Enter Predetermined Performance State by Skipping All Intermediate States Based on the Determined Utilization of the Integrated Circuit

In a confidential matter (2017) related to various patents related to semiconductor packaging technology for Latham & Watkins

In the matter of Godo Kaisha IP Bridge I v. OmniVision Technologies (Case No. 1:16-cv-00290-JFB-SRF and 5-17-cv-00778-BLF-SVK and Japan Customs with regard to Japanese Patent J3562628) and Collabo Innovations, Inc. v OmniVision Technologies (Case No. 1:16-cv-00197-JFB-SRF) – retained by Omnivision Technologies

In the matter of Magna Electronics Inc v. Valeo North America Inc, Valeo SA, Valeo GMBH, Vale Schalter und Sensoren GMBH, Connaught Electronics Ltd. (United States District Court, Eastern District of Michigan Southern Division, Case No. 2:13-cv-11376) – retained by Magna Electronics – ON GOING

EXHIBIT 2

LIST OF MATERIALS CONSIDERED BY PROFESSOR WOODWARD YANG, PH.D.

1. PRODUCED MATERIALS

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TAIWANHD-02125103	(ALL) IMP conditions Table_20150318
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TAIWANHD-02161623	DRAM Development Progress_SFTzou_v5_0524.pptx
TAIWANHD-00001025	Project M - STI 卡通圖 V4 flow.pptx
TAIWANHD-02161205	F32 Mini array and cell boundary.20160908.pptx
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UMCDOJ-01201060	MAT cell array_edge cell_corner cell_20160229.pptx
UMCDOJ-01201071	1018.lnd
UMCDOJ-01201606	7856.lnd
UMCDOJ-01201611	Xperi - UMC 14 March Meeting.pdf
UMCDOJ-01200707	1. F32s 8Gb LP4 Gross Die and Overhead Break Down.pdf
UMCDOJ-01761364	2345.lnd
UMCDOJ-01761365	34 條 TLR-supporting data.pptx
UMCDOJ-01761431	34 條 TLR 資料對應表.xlsx
UMCDOJ-01761432	複本 0.1P3 討論結果與改版原因_20171115.xlsx
UMCDOJ-01821710	5445.lnd
UMCDOJ-01821711	UMC design rule 改版紀錄_0.1P2~0.1P3.ppt
UMCDOJ-01821718	聯電 F32 design rule 改版紀錄 0.1P2~0.1P3.xlsx
UMCDOJ-02714805	3903.lnd
UMCDOJ-02714806	TLR revision 紀錄_20181129_v8.xlsx
UMCDOJ-03624886	Check.pptx
UMCDOJ-03625009	1.xlsx
UMCDOJ-03680702	Process Flow Roadmap_August 2017.pdf
UMCDOJ-03681028	AJ55 to AJ88 evolution.xlsx
UMCDOJ-03681034	CONFIDENTIAL UMC Analysis by Experts 09012018.pptx
UMCDOJ-03627678	1.xlsx
UMCDOJ-03619141	BC.pptx
UMCDOJ-03866600	DRAM Development Progress Report_May_ 2017 簡.pptx
UMCDOJ-03872983	PM1 monthly report_May Patent Filing.pptx
UMCDOJ-03937262	PM1 monthly report_Mar_2017.pptx
UMCDOJ-03953755	PM1 monthly report_Sep_2017.pptx
UMCDOJ-04204308	picture5.gif
UMCDOJ-04204309	picture6.gif
UMCDOJ-04373158	PM1 monthly report_April Patent Filing.pptx
UMCDOJ-04373161	picture1.gif
UMCDOJ-04373181	one page summary of litho 2017 0417 --- JHICC.pptx
UMCDOJ-04373182	AJ88 LITHO Pilot Summary 2017 0417 for JHICC.xlsx
UMCDOJ-04373191	recipe avaialble ratio_0320_CMP.xlsx
UMCDOJ-03625240	DRAM Development Path in UMC_20180120.pptx
UMCDOJ-03627557	DRAM PM1 研發進度 UMC_201807_40min_v3_簡.pptx
UMCDOJ-03866561	2.pdf
UMCDOJ-03866569	UMC Tool key component review.xls
UMCDOJ-03871296	Presentation 20170601 FJ.pptx
UMCDOJ-03874472	JHICC2018 budget input output plan for 3 years rolling1216-20K.XLSX
UMCDOJ-04379024	2017 NBD 方針展開_PM1_Q4_2017_CMP.xlsx
UMCDOJ-00236242	160613UMC DRAM Proposal(說明資料).pptx

Bates Number	File Name
TAIWANHD-00020874	Rexchip 25nm Flow summary 0614 Diff.xls
TAIWANHD-00035041	Rexchip 25nm Flow summary 0614 Diff.xls
TAIWANHD-00037220	Rexchip 25nm Flow summary 0614 Diff.xls
TAIWANHD-02125025	F32 25nm Flow summary-jt study.xls
TAIWANHD-02160178	F32 25nm Flow summary-jt study.xls
TAIWANHD-02125058	Meeting minute 20151207.xlsx
TAIWANHD-02125310	Rexchip 25nm Flow summary 0614 Diff.xls
TAIWANHD-02160179	F32 flow discussion.xls
TAIWANHD-02160180	Meeting minute 20151207 3.xlsx
TAIWANHD-02160192	UMC step naming_sf-1218 2.xlsx
TAIWANHD-02160143	F32 2014,2015 flow compare -20150824.xlsx
TAIWANHD-02160181	UMC step naming.xlsx
TAIWANHD-02161367	Flow Discussion_20160219_rev6.xlsx
TAIWANHD-02160144	Rexchip 25nm Flow summary 0614 Diff.xls
UMCDOJ-00158771	UMC step naming.xlsx
UMCDOJ-00158774	UMC step naming.xlsx
UMCDOJ-00366463	UMC step naming.xlsx
UMCDOJ-00680187	UMC step naming.xlsx
UMCDOJ-00841254	UMC step naming.xlsx
UMCDOJ-04088956	UMC step naming.xlsx
UMCDOJ-04089051	UMC step naming.xlsx
UMCDOJ-04362023	UMC step naming.xlsx
UMCDOJ-04396324	UMC step naming.xlsx
USD-0421725	Rexchip 25nm Flow summary 0614 Diff.xls
USD-0449310	Rexchip 25nm Flow summary 0614 Diff.xls
UMCDOJ-00236242	160613UMC DRAM Proposal(説明資料).pptx
UMCDOJ-00158770	536.lnd
UMCDOJ-00158771	UMC step naming.xlsx
TAIWANHD-02161367	Flow Discussion_20160219_rev6.xlsx
USD-0421725	Rexchip 25nm Flow summary 0614 Diff.xls
USD-0449310	Rexchip 25nm Flow summary 0614 Diff.xls
UMCDOJTT-00148191	ALDSIN BKM migration summary 10032018.pdf

In addition to the above, Professor Yang was given access to and reviewed many of the documents identified in the "Technology Transfer Package" (UMCDOJTT-00000002 – UMCDOJTT-00148378. Professor Yang reviewed a substantial portion of this production, in connection with the documents cited above and below.

Similarly, Professor Yang was given access to and reviewed many of the documents identified in Dr. Dyer's Exhibit 4. However, because some of the files listed in Dr. Dyer's Exhibit 4 were missing, corrupted or inaccessible, Prof. Yang has reviewed as many files as he could. Jinhua's counsel is in the process of requesting the government to reproduce the missing, and/or corrupted files. As such, Prof. Yang reserves the right to supplement his disclosure pending review of those reproduced files.

2. PUBLIC MATERIALS

The below documents are a representative sampling of the most important public documents Professor Yang reviewed, and are not a comprehensive list.

A. Court Materials

Title	Description
Dkt. 1	USA – Indictment of UMC, et al. [USA v. UMC 18-cr-00465]
Dkt. 2	USA – Sentencing Memorandum re UMC [USA v. UMC 18-cr-00465]
Dkt. 3	USA – Sentencing Memorandum [USA v. UMC 18-cr-00465]
Dkt. 172-35	UMC – Declaration of John Berg in Support of UMC's Motion to Dismiss Micron's 1st Amend. Complaint for Lack of Personal Jurisdiction (Redacted) [Micron v. UMC 3:17-cv-06932]
Dkt. 181-2	UMC – Declaration of John Berg in Support of UMC's Motion to Dismiss Micron's 1st Amend. Complaint for Lack of Personal Jurisdiction (Redacted) [Micron v. UMC 3:17-cv-06932]
Dkt. 230	Micron – Revised, Second Amended Complaint ("Rev. 2AC") [Micron v. UMC 3:17-cv-06932]
Dkt. 230-1	Micron – Rev. 2AC Ex. 1 [Taiwan Indictment of JT Ho] [CH] [Micron v. UMC 3:17-cv-06932]
Dkt. 230-2	Micron – Rev. 2AC Ex. 2 [Taiwan Indictment of JT Ho] [EN] [Micron v. UMC 3:17-cv-06932]
N/A	Taiwan Taichung District Procuratorate Hearing Transcript pages 1 – 72
N/A	Taiwan Taichung District Procuratorate Hearing Transcript pages 1 – 60
N/A	Taiwan Taichung District Procuratorate Hearing Transcript pages 61 – 109
N/A	05/04/2021 Letter from N. Hunter to M. Sloan re: Trade Secret 1 Documents

B. Patents and Publications

Title	Author/Owner	Publication	Year
US20090008714A1	Samsung		2007
CN107369686A	Inotera Memories Inc Micron Technology Inc		2016
US20140145268A1	Samsung		2012
US20140154882A1	Samsung		2012

Title	Author/Owner	Publication	Year
KR20130078965A	Hynix		2012
KR20160015783A	Samsung		2016
US 2015/0061134 A1	Samsung		2015
US 4,151,607	Hitachi, Ltd.		1977
US20190057870A1	Nanya		2009
US6383952	Advanced Micro Devices Inc		2001
US7349232B2	Micron Technology Inc		2008
US2015/02110	Applied Materials		2015
US 6,423,474	Micron Technology Inc		2000
US7613025B2	Micron Technology Inc		2008
US 6,822,280	Toshiba		2001
US 7,211,141	Shin Etsu Handotai Co Ltd		2004
US8508982B2	Longitude Licensing Ltd		2011
US 9,311,443	GlobalFoundries US Inc		2014
JP4361880B2	Fujitsu Microelectronics Limited		2005
US 6,438,052	NEC Electronics Corp		2002
US 8,225,255	GlobalFoundries US Inc		2012
US7723755B2	Samsung		2006
US8519462B2	Intel Corp		2011
US 6,406,971	United Microelectronics Corp.		2002
US 5,811,869	Micron Technology, Inc.		1998
US 7,349,232 B2	Micron Technology, Inc.		2008
US 6,258,732 B1	International Business Machines Corporation,		2001
US 6,383,952 B1	Advanced Micro Devices, Inc.		2002
US 6,406,971 Bl	United Microelectronics Corp.		2002
US 6,423,474 B1	Micron Technology, Inc.		2002
US 6,438,052 B1	NEC Corporation		2002
US 6,573,167 B2	Texas Instruments Incorporated		2003
US 7,183,603 B2	Samsung Electronics Co., Ltd.		2007
US 7,736,819 B2	Pixer Technology Ltd.		2010
US 8,058,138 B2	Micron Technology, Inc.		2011
US 8,225.255 B2	International Business Machines Corporation		2012
US 8,312,394 B2	Synopsys, Inc.		2012
US 8,486,801 B2	Inotera Memories, Inc.		2013
US 8,524,601 B2	Mitsubishi Electric Corporation		2013

Title	Author/Owner	Publication	Year
US 9,136,331 B2	Micron Technology, Inc.		2015
US 9,311,443 B2	GLOBALFOUNDRIES INC.		2016
US 9,589,799 B2	Lam Research Corporation		2017
US 9,772,555 B2	SAMSUNG ELECTRONICS CO . LTD.		2017
US 10,103,152 B2	SAMSUNG ELECTRONICS CO . LTD.		2018
US 2009/0061329 A1	ELPIDA MEMORY, INC.		2009
US 2014/0145268 A1	SAMSUNG ELECTRONICS CO . LTD.		2014
US 2014/0154882 A1	SAMSUNG ELECTRONICS CO . LTD.		2014
US 2015/0061134 A1	EUN-OK LEE, et al.		2015
US 2015/0200110 A1	Applied Materials, Inc.		2015
US 2015/0311297 A1	SAMSUNG ELECTRONICS CO . LTD.		2015
US 2015/0333069 A1	SK hynix Inc.		2015
US 2016/0035788 A1	SAMSUNG ELECTRONICS CO . LTD.		2016
US 7,349.232 B2	Micron Technology, Inc.		2008
A 6F2 Buried Wordline DRAM Cell for 40nm and Beyond	T. Schloesser, et al.	IEEE	2008
8Gb B-die DDR4 SDRAM 78FBGA with Lead-Free & Halogen-Free (RoHS compliant)	Samsung	Samsung	2017
DRAM - Circuits Organization Interfaces	Shih-Lien Lu	IEEE Microarchitecture Conference	2016
A multigigabit DRAM technology with 6F2 open-bitline cell, distributed	Tsugio Takahashi et al.	IEEE Journal of Solid-State Circuits 36(11):1721 - 1727	2001

Title	Author/Owner	Publication	Year
overdriven sensing, and stacked-flash fuse			
High-Density Low-Power-Operating DRAM Device Adopting 6F2 Cell Scheme with Novel S-RCAT Structure on 80nm Feature Size and Beyond	H.J. Oh, et al.	Proceedings of ESSDERC, Grenoble, France	2005
Hynix DRAM layout, process integration adapt to change	Ron Maltiel	https://www.maltiel.com/	2012
20nm DRAM: A new beginning of another revolution	J.M. Park et al.	IEDM15-676	2015
1T-1C Dynamic Random Access Memory Status, Challenges, and Prospects	Alessio Spessot et al.	IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 67, NO. 4	2020
DRAM Device Organization: Basic Circuits and Architecture	Bruce Jacob, et al.	Basic Circuits and Architecture	
DRAM Circuit Design: Fundamental and High-Speed Topics	Brent Keeth et al.	IEEE Press Series on Microelectronic Systems	2007
DRAM Nonvolatile Memory SRAM	Ron Maltiel	Semiconductor Technology Online	
Introduction to DRAM (Dynamic Random-Access Memory) - Technical Articles		https://www.allaboutcircuits.com/technical-articles/introduction-to-dram-dynamic-random-access -memory/	
반도체 메모리 구조의 이해	Koo, Bon-Jae	KIPO	2007
6F2 개발 후 EUV Lithography 시작	게시일	https://go2origin.wordpress.com/author/go2origin/	2015
Next generation DRAM technology that promotes large capacity without relying on miniaturization	Akira Fukuda	PC Watch	2018
DRAM	SK hynix	SK Hynix	2012

Title	Author/Owner	Publication	Year
Technology			
DRAM makers find new processes for sub-nm DRAM cells	Jeongdong Choe	EET Asia	2013
Dynamic RAM Technology Advancements	Muzaffer A.Siddiqi	Multiple Patterning - wikipedia for fine pitch photolithography techniques	2013
Technology for sub-50nm DRAM and NAND Flash Manufacturing	Kinam Kim	IEEE	2005
NAND FLASH MEMORY TECHNOLOGIES	SEIICHI ARITOME	IEEE Press Series on Microelectronic Systems	2016
Semiconductor Reliability and Quality Assurance– Failure Mode, Mechanism and Analysis (FMMEA)	EDN	https://www.edn.com/semiconductor-reliability-and-quality-assurance-failure-mode-mechanism-and-analysis-fmmea/	2014
ENABLING ADVANCED WAFER PROCESSING WITH NEW MATERIALS	ASM	ASM International Analyst and Investor Technology Seminar	2017
Novel and cost-effective multiple patterning technology by means of invisible SiOxNy hardmask	Linus Jang et al.	PROCEEDINGS OF SPIE	2014
A New Method to Characterize Conformality of BARC Coatings	Runhui Huang, et al.	Proceedings of SPIE, vol. 5753	2005
Bottom Anti-Reflective Coatings (BARCs) for 157-nm!Lithography	Liu He et al.	Proceedings of SPIE: Advances in Resist Technology and Processing XXI, vol. 5376	2004
Virtual fabrication using directed self-assembly for process optimization in a 14-nm dynamic random access memory	Mattan Kamon et al	J. Micro/Nanolith. MEMS MOEMS 15(3), 031605	2016
A Study of Wiggling AA	QingPeng Wang, et al.	Coventor Inc., a Lam Research Company	

Title	Author/Owner	Publication	Year
modeling and Its Impact on the Device Performance in Advanced DRAM			
Double patterning lithography: double the trouble or double the fun?	Paul Zimmerman	SPIE Newsroom	2009
Speeding Up Process Optimization With Virtual Processing	Joseph Ervin	Lam Research	2020
Double Patterning for Memory ICs	Christoph Ludwig and Steffen Meyer	Q-CELLS SE, Bitterfeld-Wolfen Germany	2011
DRAM Scaling Challenges Grow	Mark Lapedus	SemiconductorEngineering	2019
Fill/Cut Self-Aligned Double-Patterning	David Abercrombie	SemiconductorEngineering	2016
⋯ and optoelectronic materials by Atomic Layer Deposition: An overview with special emphasis on recent progress in processing of high‐k dielectrics and other oxide ⋯	L Niinistö et al.	phys. stat. sol. (a) 201, No. 7, 1443–1452	2004
Chapter 4 Mass-Production Memories (DRAM and Flash)	Cheol Seong Hwang, et al.		2014
Dielectric Barrier, Etch Stop, and Metal Capping Materials for State of the Art and beyond Metal Interconnects	Sean W. King	ECS J. Solid State Sci. Technol. 4 N3029	2015
Exposed Pattern Interaction of Litho-cure-litho-etch Process in Computational Lithography	Sang-Kon Kim	Journal of the Korean Physical Society, Vol. 59, No. 2,	2011

Title	Author/Owner	Publication	Year
Mask contribution on CD & OVL errors budgets for Double Patterning Lithography	I. Servina, et al.	25th European Mask and Lithography Conference,	2009
Correlation between pattern density and linewidth variation in silicon photonics waveguides	YUFEI XING, et al.	Optical Society of America	2020
Managing Lithographic Variations in Design, Reliability, and Test Using Statistical Techniques	Aswin Sreedhar	Open Access Dissertations. 358.	2011
Accurate mask registration on tilted lines for 6F2 DRAM manufacturing	Roeth, K. D., et al.	SPIE Photomask Technology	2015
Time Diversification & Reference point	Ted Lim	https://tedvc.com/	2019
Memory Trends and Implications for Lithography and DSA Technology	Linda K. Somerville, et al.	Micron Technology, Inc.	2015
Micron's 1x DRAMs Examined	Jeongdong Choe	EE Times	2018
Development of high-performance multi-layer resist process with hardening treatment	Ono, Yoshiharu, et al.	Proc. SPIE 6519, Advances in Resist Materials and Processing Technology XXIV, 65192O	2007
Multiple patterning	Wikipedia	Wikipedia	2020
New Patterning Paradigm?	Mark Lapedus	SemiconductorEngineering	2015
Overview: continuous evolution on double-patterning process	Yaegashi, Hidetami, et al.	Proc. SPIE 8325, Advances in Resist Materials and Processing Technology XXIX, 83250B	2012
Pattern dependent profile distortion during plasma etching of high aspect ratio features in SiO2	Shuo Huang, et al.	J. Vac. Sci. Technol. A 38, 023001	2020

Title	Author/Owner	Publication	Year
Advanced self-aligned double patterning development for sub-30-nm DRAM manufacturing	Troy Wang	Proceedings of SPIE - The International Society for Optical Engineering	2009
22nm half-pitch patterning by CVD spacer self alignment double patterning (SADP) - art. no. 69244E	Chris Bencher, et al.	Proceedings of SPIE - The International Society for Optical Engineering	2008
Samsung Tech Conference 2006(2D pattern Design and application for 80nm node devices and beyond)	Ted Lim	https://tedvc.com/6	2014
Novel Flowable CVD Process Technology for sub-20nm Interlayer Dielectrics	Honggun Kim, et al.	IEEE	2012
A spacer-on-spacer scheme for self-aligned multiple patterning and integration	Angélique Raley, et al.	SPIE The International Society for Optics and Photonics	2016
Self-Aligned Double Patterning—Part Deux	David Abercrombie	SemiconductorEngineering	2014
Self-Aligned Double Patterning, Part One	David Abercrombie	SemiconductorEngineering	2014
Semiconductor Reliability and Quality Assurance–Failure Mode, Mechanism and Analysis (FMMEA)	EDN	https://www.edn.com/semiconductor-reliability-and-quality-assurance-failure-mode-mechanism-and-analysis-fmmea/	2014
A spacer patterning technology for nanoscale CMOS	Yang-Kyu Choi et al.	IEEE Transactions on Electron Devices 49(3):436 - 441	2002
Sentaurus TCAD Industry-Standard Process and Device Simulators	Synopsys	Synopsys	2012
Implementation and Development of the	T. Valente, et al.	JTTEE5 14:462-470	2004

Title	Author/Owner	Publication	Year
Incremental Hole Drilling Method for the Measurement of Residual Stress in Thermal Spray Coatings			
Review Article: Stress in thin films and coatings: Current status, challenges, and prospects	Grégory Abadias, et al.	J. Vac. Sci. Technol. A 36, 020801	2018

EXHIBIT 3

GLOSSARY OF TERMS USED IN PROFESSOR WOODWARD YANG'S DISCLOSURE

1. DRAM: Acronym for Dynamic Random Access Memory.

2. DRAM Cell Structure: The physical 3D details and material composition of the DRAM cell including the active area, buried wordline, bitline, access transistor, contact structures, and storage capacitor.

3. DRAM Cell Array (a/k/a DRAM mat): An array of DRAM cells including dummy rows and columns and possible subwordline drivers depending on the architecture.

4. DRAM Periphery Interface Circuitry: All other circuitry outside the DRAM cell array which is required for the proper functioning of DRAM.

5. DRAM Chip: Fully integrated DRAM cell array + DRAM periphery interface circuitry.

6. DRAM Chip Mask Layers: Actual photolithography masks used in DRAM manufacturing process.

7. DRAM Manufacturing Process: The detailed sequential step-by-step process for manufacturing a wafer of DRAM chips (does not include testing, repair, or packaging) and based on specific semiconductor manufacturing equipment.

8. Recipe: The detailed instructions for performing a semiconductor manufacturing process step on a wafer which may be highly equipment specific.